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EMBER® EM35X NCP BREAKOUT BOARD TECHNICAL SPECIFICATION

The Silicon Labs' Ember EM35x Network Co-Processor (NCP) Breakout Board contains the hardware peripherals for the development and deployment of a low-data-rate, low-power ZigBee application on a host micro interfacing via EZSP protocol to the EM300 series NCPs. The NCP Breakout Board supports SPI and UART EZSP interfaces for development flexibility.

Modules separately contain the EM35x NCP and the HOST microcontroller to allow for higher degrees of freedom during application development. The modules are connected to the NCP Breakout Board though robust connectors.

The EM35x NCP Breakout Board hardware stimuli include a temperature sensor, two buttons, a piezo buzzer, two LEDs, and a 1.6" x 1.8" through-hole prototyping area. The EM35x NCP Breakout Board also contains a USB transceiver with USB connector, a RS-232 transceiver with DB-9 connector, Data Emulation Interface (DEI), Packet Trace Port programming interface, and regulated power planes. The EM35x NCP Breakout Board also includes an optional host interface to 2 Mbit external DataFlash in support of the ZigBee OTA upgrade cluster for over-the-air (OTA) application bootloader purposes.

You can obtain the EM35x NCP Breakout Board voltage supply from one of four sources: Debug Adapter (ISA3) (through the Packet Trace Port), external VDC supply, USB port, or AAA battery pack. The various voltage supplies offer a degree of flexibility when testing different network topologies.

This document provides the technical specification for the EM35x NCP Breakout Board. It describes the board-level interfaces as well as the key performance parameters. In addition, it provides the necessary information for developer to validate their application designs using the EM35x NCP Breakout Board.

New in This Revision

Document renumbering.

Contents

1 EM35x NCP Breakout Board Features

The EM35x NCP Breakout Board offers:

- Configurable hardware support for application development

  Temperature sensor (connects to host GPIO)
  Two buttons (connect to host GPIO)
  Piezo buzzer (connect to host GPIO)
  Two LEDs (connect to host GPIO)
- RS-232 transceiver with DB-9 connector for serial communication (with hardware (HW) handshake support)
- USB transceiver with USB connector (Type B)
- 2 MB external DataFlash for ZigBee OTA Profile support
- Control Interface for the EM35x Radio Communications Module (RCM)

  RCM RESET and Bootload buttons
  Voltage Supply connection (V_NCP_EN)
- Control Interface for the Host Module

  RCM RESET and Bootload buttons
  Voltage Supply connection (V_HOST_EN)
- 1.6" x 1.8", 0.1" pitch prototyping area
- 26-pin, 0.1" pitch, dual-row logic-analyzer shrouded connector
- 10-pin, 0.05" pitch, dual-row Packet Trace Port connector
- 12-pin, 0.1” pitch, dual-row, data emulation interface (DEI) with configuration header
- 14-pin, 0.05” pitch, single-row along with a 19-pin 0.05” pitch, single-row, board-to-board connector for the module
- 16-pin, 0.1” pitch, single-row along with a 20-pin 0.1” pitch, single-row, board-to-board connector for the host module
- Selection pins for DC power source selection (either external DC power supply, USB, Debug Adapter (ISA3), or AAA battery pack). LEDs indicate which power supply has been selected.
- 2-pin module VDC pin for connection of an ammeter for EM5x module current measurements
- 2-pin module VDC pin for connection of an ammeter for host module current measurements
- 2-pin jumpers for each of the HW application peripherals, buzzer, buttons, piezo, temperature sensor, and LEDs
- 2-pin jumpers for connection to TTL UART for either the EM35x UART (SC1) or host UART2. The selection jumpers route signals (RXD, TXD, nRTS, and nCTS) allow access to the TTL levels.

Table 1 lists the DC electrical characteristics of the EM35x NCP Breakout Board.

Table 1. DC Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit
VDD supply				
External DC Supply (J1 / J32)	4		20	V
USB Host	4.5	5		V
Debug Adapter	3.1	3.3V	3.5	V
Battery	2.1		3.6	
External DC supply (J3.2)	3.1	3.3	3.5	V
Current draw (peripherals)				
Piezo buzzer			10	mA
Buttons (enabled)			6	mA
Temperature sensor (enabled)			5	mA
Current draw (miscellaneous)				
RS-232 transceiver			4	mA
USB transceiver			15	mA
LDO distribution			10	mA
Operating temperature	0		+ 55	C

2 Components

Figure 1 illustrates the components on layer 1 (top side).

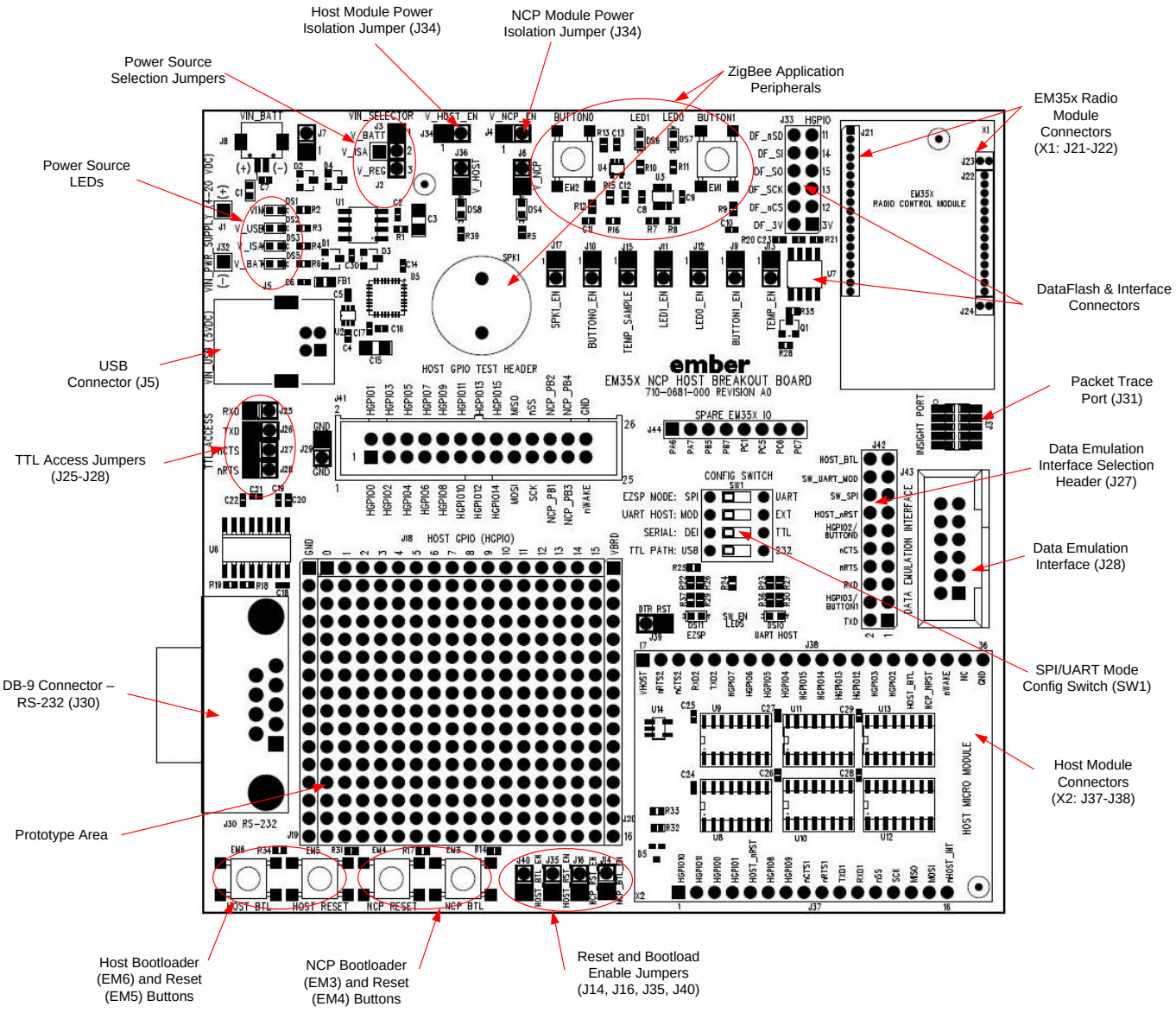

Figure 1. Assembly Print for Layer 1

2.1 Power Supply and Distribution

The EM35x NCP Breakout Board can be powered from one of five sources:

- 4 V to 20 V External DC Power supply (Positive connected J1 and Ground connected to J32)
- Battery pack connector (J8)
- USB Host (J5, via Wall wart or PC connection)
- Debug Adapter (ISA3) (through Packet Trace Port, J31)
- 2.1 to 3.6 V External DC Power supply (Positive connected to J3.2 and Ground connected to J32)

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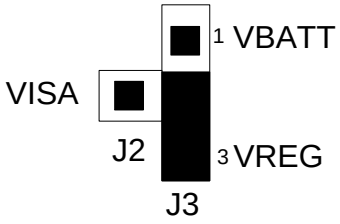
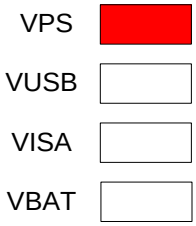
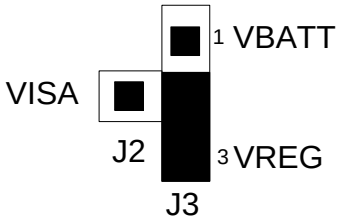
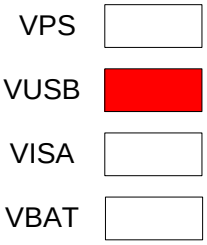
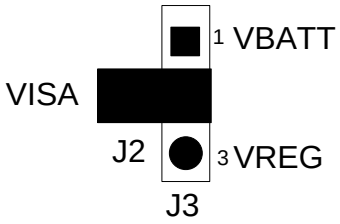
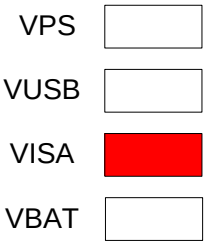
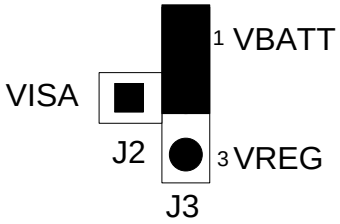
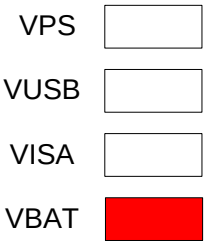
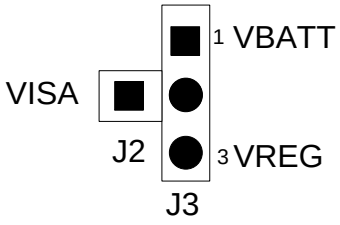
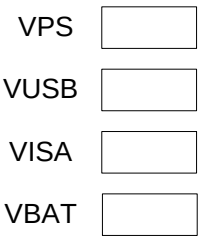
The EM35x NCP Breakout Board contains power source selection jumpers (J2 and J3) which allows only one DC source to power the board. This eliminates the possibility of overcurrent resulting from power supply contention. Table 2 illustrates the connection scheme and LED indication for each power source.

Table 2. Power Supply connections

Power Source	Selection Scheme (J2 and J3)	LED Indicator
High Voltage External supply (4 V to 20 V) *Connect VDD to J1 and GND to J32.*		
USB Host *Connect USB cable to J5.*		
Debug Adapterr (ISA3) *Connect Debug Adapter (ISA3) to J31.*		
Battery pack *Connect AAA battery pack (supplied by Silicon Labs) to J8.*		
Low Voltage External DC supply (3.1 to 3.5) *Connect directly to J3.2 with Ground connected to J32.*		

2.1.1 External DC Power Supply (J1 and J32 or J3.2 and J32)

The EM35x NCP Breakout Board allows two easy to use connections to an external power supply.

- The first connection (Low Voltage) allows for a 3.1 to 3.5 V DC external supply to be connected to J3.2 (positive) and J32 (Ground). The power supply should be able to source up to 250 mA at the set voltage. When using a power supply in this mode, there should be no jumpers on J2 or J3 as shown in Table 2.
- The second connection (High Voltage) allows for a 4 V to 20 V DC external supply to be connected to J1 (positive) and J32 (Ground). The power supply should be able to source up to 300 mA at the set voltage. When using a power supply in this mode, there should be a jumper connecting J3.3 and J3.2 as shown in Table 2.

2.1.2 Battery Connector (J8)

The 2-pin, keyed battery connector (Hirose, P/N: DF13-2P-1.25H(50)) allows for connection to a DC power supply or battery pack. The EM35x NCP Breakout Board is shipped with a 2-AAA battery pack with appropriate mating connector for easy attachment. Batteries are sold separately. When using a battery pack, a jumper must be connected between J3.1 and J3.2 as shown in Table 2.

2.1.3 Packet Trace Port (J8)

The EM35x NCP Breakout Board can also be powered from a Debug Adapter (ISA3). To enable this power supply, simply connect the Debug Adapter (ISA3) to the Packet Trace Port (J8) and connect the power selection jumper between J2 and J3.2 as shown in Table 2. In addition, the Debug Adapter (ISA3) selection toggle switch must be put in the INT. The Debug Adapter (ISA3) provides a target voltage of 3.3V and sources as much as 250 mA. See document TS7, *Debug Adapter (ISA3) Technical Specification,* for more details on the Debug Adapter (ISA3).

Note: If the Debug Adapter (ISA3) is connected directly to the Packet Trace Port on the Module, the jumpers at J4 and J34 must be connected as well as the jumper across J2 and J3.2.

2.1.4 USB Host (J5)

The EM35x NCP Breakout Board can also be powered by a USB Host (PC or Silicon Labs-supplied USB power supply). To operate in this mode, a USB Host must be connected to J5 and the power selection jumper must be connected between J3.1 and J3.2 as shown in Table 2.

2.2 NCP Current Measurements

To allow for NCP current measurements, the EM35x NCP Breakout Board isolates the NCP module VDD power supply from the regulated power domain on the Breakout Board. The only connection point between the NCP module power supply and the Breakout Board supply is through the V_NCP_EN header (J4). Remove J4 and place an ammeter across this jumper to measure the NCP current draw.

2.3 Host Current Measurements

To allow for Host current measurements, the EM35x NCP Breakout Board isolates the Host module VDD power supply from the regulated power domain on the Breakout Board. The only connection point between the Host module power supply and the Breakout Board supply is through the V_HOST_EN header (J34). Remove J34 and place an ammeter across this jumper to measure the Host current draw.

2.4 Deep Sleep Testing of the EM35x Module

To perform accurate deep sleep measurements of the EM35x NCP, configure the EM35x NCP Breakout Board as follows:

- Remove J4 and place ammeter across this jumper.

- Remove J6 so the V_NCP LED DS4 is not driven. If supplying voltage through J8 battery connector, also remove J7 so the V_BATT LED DS5 is not driven.
- Remove J33 jumpers to isolate DataFlash IC from circuit.
- Issue "shutdown" in nodetest.
- Once command is issued and node is asleep, remove J25-J28 (TTL jumpers).
- Make sure the Packet Trace Port cable, DEI cable, and RS-232 cable are all detached from the Breakout Board.

This connection scheme offers the highest degree of power supply flexibility. Wake the EM35x NCP from deep sleep by pressing the NCP reset button.

Note: The use of virtual UART port 4900 is not recommended when interfacing to nodetest for deep sleep testing, since this does not allow for proper configuration of the EM35x for deep sleep measurements. Therefore, please use either pass-through UART port 4901, USB, or RS-232 to interface to the nodetest application.

2.5 ZigBee Application Peripherals

As previously mentioned, the EM35x NCP Breakout Board offers six host peripherals to assist in ZigBee application development including:

- Temperature sensor
- Two (2) “normally open” buttons
- 4 kHz piezo buzzer
- Two (2) LEDs
- External DataFlash

Each peripheral connects to a host GPIO through a two-pin peripheral header. Because each peripheral header on the EM35x NCP Breakout Board ships with a jumper in place, the peripherals default to “HW Enabled.” If application development does not require the peripheral, simply remove the jumper.

Note: Each peripheral consumes power. Be sure to factor this into the current consumption equations when testing the module in deep sleep mode or if using the battery pack to power the Breakout Board.

2.5.1 Temperature Sensor (U4)

The temperature sensor is an off-the-shelf component from National Semiconductor (MFG P/N: LM20BIM7). The temperature sensor requires an enable signal to be asserted (active high) prior to generating an analog voltage proportional to the ambient temperature of the EM35x NCP Breakout Board. Therefore, two host GPIO signals, HGPIO7 and HGPIO8, are routed to pin 2 of peripheral headers J13 and J15, respectively.

- HGPIO7 enables the temperature sensor when asserted (active high), when a jumper is installed at J13.
- HGPIO8 contains the analog temperature information from the sensor, when it is enabled and a jumper is installed at J15.

The temperature sensor output is scaled to between 0 and 1.2 V through a resistive voltage divider. If you want to connect a temperature sensor from a different manufacturer, scale the output in a similar manner.

The EM35x NCP Breakout Board is shipped with a jumper installed at J13 and J15. If the jumpers are removed, a different compatible device can be attached to pin 2 of both J13 and J15.

For more information on the temperature sensor, refer to its data sheet (http://www.ti.com/product/LM20).

2.5.2 Buttons (EM1, EM2)

Two programmable, normally-open buttons are provided for software debugging and application development. When either button is pressed, the connected net is driven low. A single-pole RC filter minimizes the effects of switching noise.

These buttons map to the backchannel button commands as follows:

- EM2: controlled by the `button 0` command
- EM1: controlled by the `button 1` command

For information about the `button` command, see document UG110, the *EM35x Development Kit User Guide*.

Two host GPIO signals, HGPIO3 and HGPIO2, are routed from the EM35x Module to pin 2 of peripheral headers J9 and J10, respectively. In the default configuration of the EM35x NCP Breakout Board, jumpers are positioned across J9 and J10 to enable buttons EM1 and EM2, respectively. If the jumpers are removed, different compatible devices can be attached to pin 2 of breakout headers J9 and J10 instead of the buttons.

2.5.3 Buzzer (SPK1)

A programmable buzzer is provided for software debugging and application development. A host GPIO signal, HGPIO4, is routed to pin 2 of peripheral header J17. In the default configuration of the EM35x NCP Breakout Board, a jumper is positioned across J17 to enable use of the buzzer. The buzzer installed on the EM35x NCP Breakout Board is from CUI (MFG P/N: CEP-1160). For more information on the buzzer, refer to its datasheet (http://www.cui.com/Product/Resource/PDFRedirect/110/CEP-1160.pdf).

2.5.4 LEDs (DS6 and DS7)

The EM35x NCP Breakout Board contains two LEDs for software debugging and application development. Each LED is buffered (non-inverting) to allow for connection to any host GPIO. Two host GPIOs, HGPIO0 and HGPIO1, are routed to pin 2 of headers J12 and J11 respectively. To turn on DS7 (RED) from the host module, install a jumper at J12, configure HGPIO0 as an output and drive it low. To turn on DS6 (GREEN), install a jumper at J11, configure HGPIO1 as an output and drive it low.

2.5.5 External DataFlash (U7)

The external DataFlash is an off-the-shelf component from Atmel (MFG P/N: AT45DB021D-SSH-B). The DataFlash is used in cases where ZigBee OTA Profile application bootloader is required for the host. The DataFlash is connected to the host module through jumper block J33. The EM35x NCP Breakout Board is shipped with jumpers installed in a disconnected state at J33. If all six jumpers are installed properly at J33, the external DataFlash connects to the host for application bootloading. Figure 2 illustrates the J33 jumper configuration for the DataFlash interface.

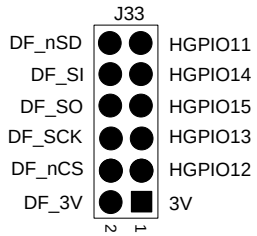


Figure 2. Jumper for DataFlash connections

For more information on the DataFlash, refer to its datasheet (http://www.atmel.com/Images/doc3638.pdf).

2.6 EZSP and Serial Mode Configuration Switch (SW1)

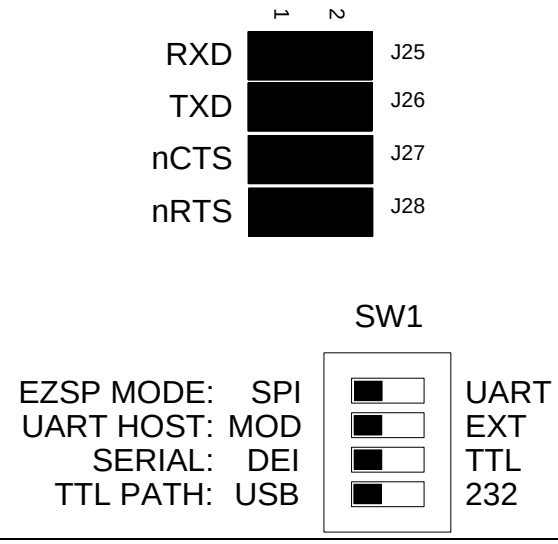
To enhance the software development experience, the EM35x NCP Breakout Board allows for EZSP interfaces between the EM35x NCP and a host via both SPI and UART (either to the host module or an external host). A configuration switch (SW1) is used to set up EZSP mode and serial communication paths. Access to either the EM35x SC1 UART or host UART1 is available directly from the EM35x NCP Breakout Board or by telnetting into port 4901 of a Debug Adapter (ISA3) connected to an Ethernet network. On the EM35x NCP Breakout Board, it is available as RS-232, USB and TTL-compliant signal levels.

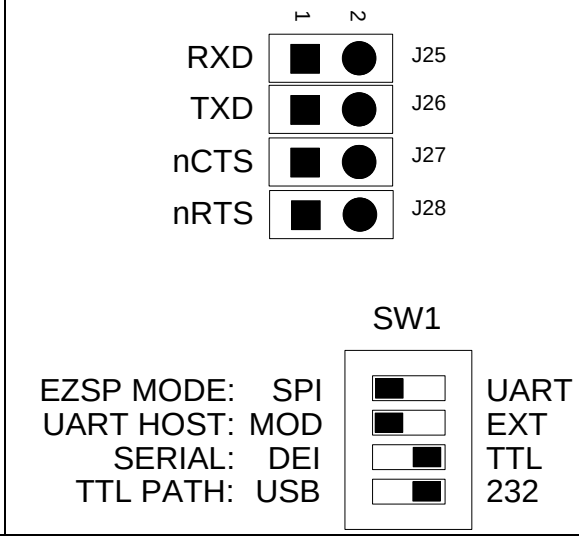
To minimize current consumption and allow for the different configuration options, the EM35x NCP Breakout Board individually routes the TTL UART signals RXD, TXD nCTS, and nRTS to pin 2 of headers J25, J26, J27, and J28 respectively. To route the UART signals to the USB transceiver, move SW1 Serial to TTL and TTL Path to USB. To route the UART signals to the RS-232 transceiver, move SW1 Serial to TTL and TTL Path to 232. To access TTL signals, move SW1 Serial to TTL, remove the jumpers on J25, J26, J27 and J28 and connect to pin 2 of these jumpers. To route the UART signals to DEI, move SW1 Serial to DEI and place jumpers on the DEI jumper connector (J42) as summarized below and shown in Figure 3.

- TXD: J27.1 to J27.2
- RXD: J27.5 to J27.6
- nRTS: J27.7 to J27.8
- nCTS: J27.9 to J27.10

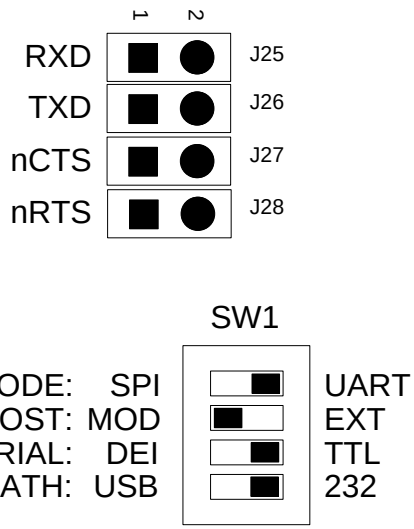
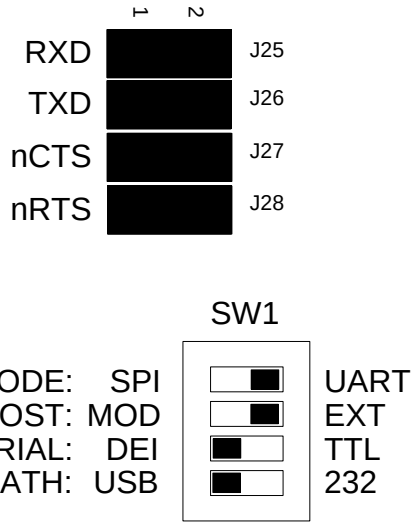
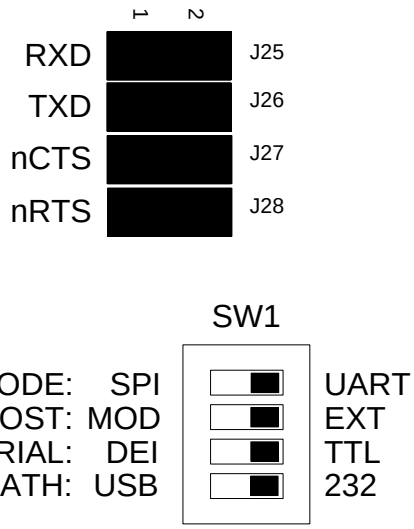
Each SW1 configuration is shown in Table 3. TTL Access Jumper configuration is shown in Table 4.

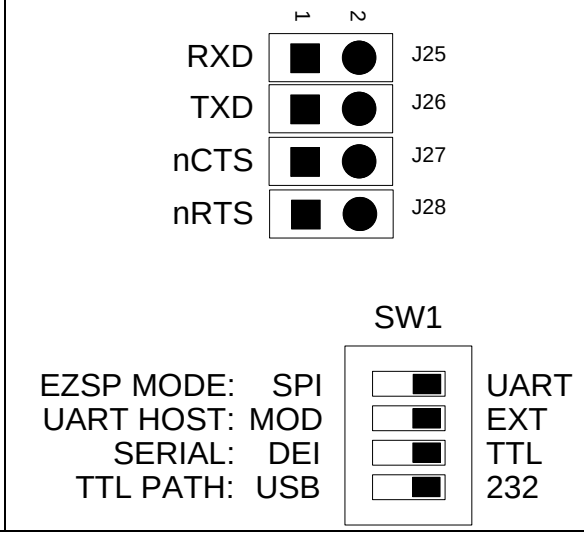
Table 3. EZSP and Serial Configuration Switch

UART Path	Selection Scheme (J22, J25, J24, and J26)
EZSP SPI Mode, Host UART2 to DEI *Connect Debug Adapter (ISA3) DEI cable to J31.*	

UART Path	Selection Scheme (J22, J25, J24, and J26)
EZSP SPI Mode, Host UART2 to RS-232	
EZSP SPI Mode, Host UART2 to USB	
EZSP SPI Mode, Host UART2 to TTL	

UART Path	Selection Scheme (J22, J25, J24, and J26)
EZSP UART Mode to Host Module, Host UART2 to DEI *Connect Debug Adapter (ISA3) DEI cable to J31.*	
EZSP UART Mode to Host Module, Host UART2 to RS-232	
EZSP UART Mode to Host Module, Host UART2 to USB	

UART Path	Selection Scheme (J22, J25, J24, and J26)
EZSP UART Mode to Host Module, Host UART2 to TTL	
EZSP UART Mode to External Host, NCP UART to DEI *Connect DEI cable to J31.*	
EZSP UART Mode to External Host, NCP UART to RS-232	

UART Path	Selection Scheme (J22, J25, J24, and J26)
EZSP UART Mode to External Host, NCP UART to USB	
EZSP UART Mode to External Host, NCP UART to TTL	

Note: To connect to the UART through a Debug Adapter (ISA3), the Debug Adapter (ISA3) must be connected to an Ethernet connection. It can be accessed by issuing “Serial 1” within the Console view of the Ember Desktop or by telnetting to Port 4901.

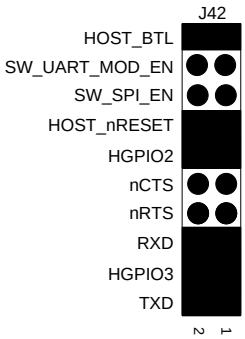
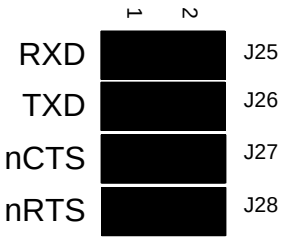
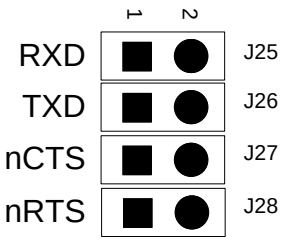


Figure 3. Jumper Settings Required for EM35x SC1 UART Access by Debug Adapter (ISA3)

Table 4. TTL Access Jumpers

Configuration	Selection Scheme (J25, J26, J27, and J28)
UART via USB or Serial	
UART via TTL Access	

2.7 Data Emulation Interface (J43)

The 12-pin, dual-row, data emulation interface contains 4 host GPIO signals, 4 host or EM35x NCP UART signals, and 2 DEI control pins, as well as voltage (VBRD) and ground (GND) connections. When connected to the Debug Adapter (ISA3), the connector provides additional debug features to software developers.

One feature involves the port 4901 UART connection through Debug Adapter (ISA3). To enable the UART connection to either the host or the EM35x NCP UART signals, configure SW1 for DEI mode as shown in Table 3 and install four jumpers on J42 as shown in Figure 3 for nCTS, nRTS, RXD, and TXD.

Another feature involves manipulation of BUTTON0 and BUTTON1 GPIO signals. To enable GPIO manipulation of BUTTON0 and BUTTON1, install jumpers on J42 at HGPIO2 and HGPIO3, respectively.

2.8 EM35x Module Interface Connector (J21-J24)

Two single-row, 0.05” pitch, connectors make up the EM35x module interface to the EM35x NCP Breakout Board. In addition, two single-row, guide connectors assist with connecting the EM35x module to the EM35x NCP Breakout Board. The board-to-board connector scheme allows access to all EM35x GPIO as well as nRESET and the JCLK signals. The connector is illustrated in Figure 4, while the dimensions are shown in Figure 5.

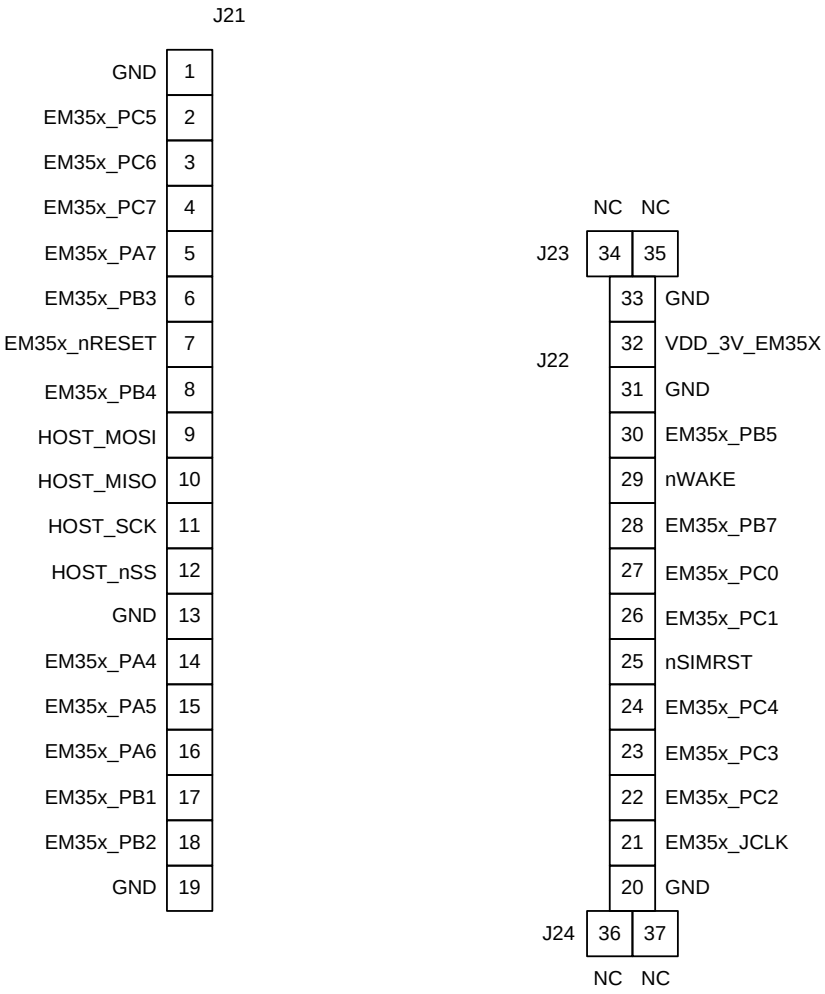


Figure 4. Board-to-Board Connector for the EM35x Module

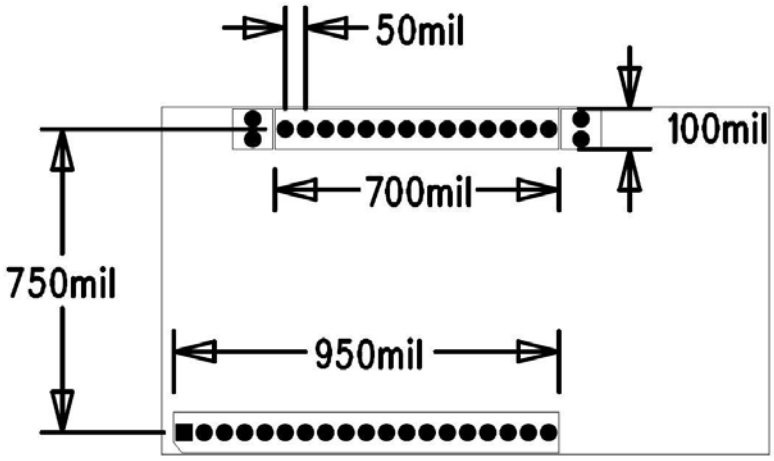


Figure 5. Board-to-Board Connector Dimensions for the EM35x Module

Table 5 describes the pinout and signal names at J21-J24. The EM35x UART1 signals (PB1, PB2, PB3, PB4) are exposed on the EM35x NCP Breakout Board at the 26-pin, dual row, 0.1” pitch GPIO connector (J41) for application development.

Note: Custom EM35x modules (not shipped with development kits) containing external DataFlash should NOT be connected to the EM35x NCP Breakout Board, as the EM35x SPI1 is used for the EZSP SPI interface.

For more information on the alternate functions of the GPIO connector, refer to document 120-035X-000, the *EM351/7 Data Sheet*.

Table 5. Pinout and Signal Names of the NCP Interface Connector

Pin #	Signal name	Direction[2]	Connector	Description
1	GND	Power	J21	Ground Connection
2	PC5	I/O	J21	EM35x GPIO
3	PC6	I/O	J21	EM35x GPIO
4	PC7	I/O	J21	EM35x GPIO
5	PA7	I/O	J21	EM35x GPIO
6	PB3	I/O	J21	EM35x GPIO
7	nRESET	I/O	J21	Active low chip reset (internal pull-up on EM35x)
8	PB4	I/O	J21	EM35x GPIO
9	PA0	I/O	J21	EM35x GPIO
10	PA1	I/O	J21	EM35x GPIO
11	PA2	I/O	J21	EM35x GPIO
12	PA3	I/O	J21	EM35x GPIO
13	GND	Power	J21	Ground connection
14	PA4	I/O	J21	EM35x GPIO
15	PA5	I/O	J21	EM35x GPIO
16	PA6	I/O	J21	EM35x GPIO
17	PB1	I/O	J21	EM35x GPIO
18	PB2	I/O	J21	EM35x GPIO
19	GND	Power	J21	Ground connection
20	GND	Power	J22	Ground connection
21	JCLK	Input	J22	JTAG interface, serial clock
22	PC2	I/O	J22	EM35x GPIO
23	PC3	I/O	J22	EM35x GPIO
24	PC4	I/O	J22	EM35x GPIO
25	PB0	I/O	J22	EM35x GPIO
26	PC1	I/O	J22	EM35x GPIO
27	PC0	I/O	J22	EM35x GPIO
28	PB7	I/O	J22	EM35x GPIO
29	PB6	I/O	J22	EM35x GPIO
30	PB5	I/O	J22	EM35x GPIO
31	GND	Power	J22	Ground connection
32	VDD	Power	J22	2.1 to 3.6V Module Power Domain
33	GND	Power	J22	Ground connection
34	NC	N/A	J23	Not connected; guide pin
35	NC	N/A	J23	Not connected; guide pin

Pin #	Signal name	Direction[2]	Connector	Description
36	NC	N/A	J24	Not connected; guide pin
37	NC	N/A	J24	Not connected; guide pin

[2] with respect to the RCM

2.9 Host Module interface connector (J37-J38)

Two single-row, 0.1” pitch, connectors make up the host module interface to the EM35x NCP Breakout Board. The board-to-board connector scheme allows access to 16 host GPIO. The connector is illustrated in Figure 6, while the dimensions are shown in Figure 7.

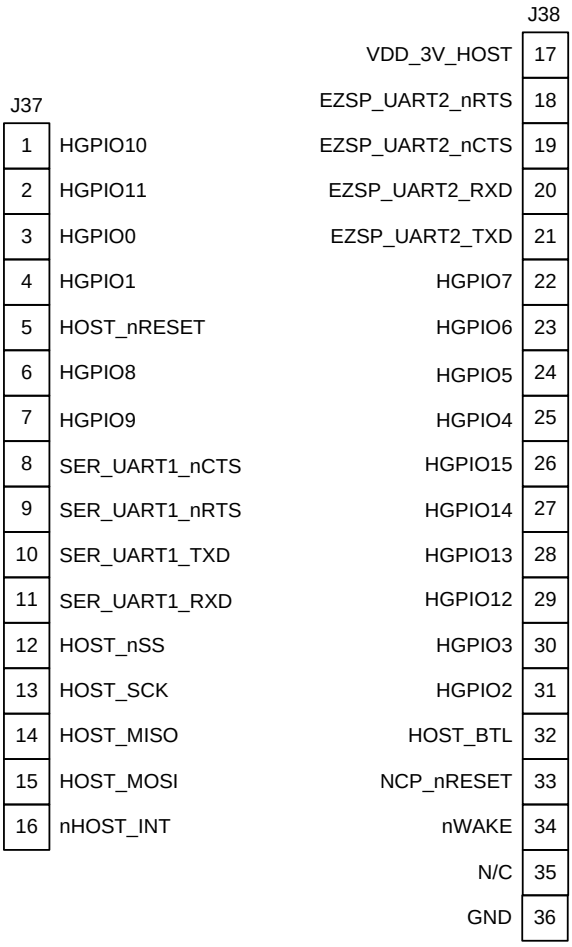


Figure 6. Board-to-Board Connector for the Host Module

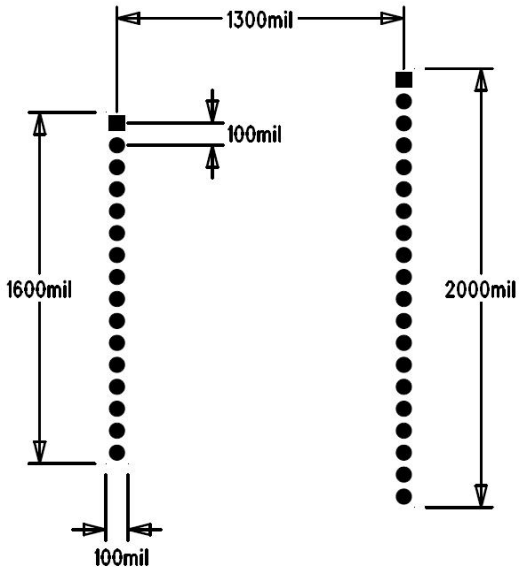


Figure 7. Board-to-Board Connector Dimensions for the Host Module

Table 6 describes the pinout and signal names at both J37 and J38. 16 host GPIOs are exposed on the EM35x NCP Breakout Board at the 26-pin, dual row, 0.1" pitch GPIO connector (J41) for application development.

For more information on the alternate functions of the GPIO connector, refer to the data sheet for the host microprocessor included on the host module.

Table 6. Pinout and Signal Names of the Host Interface Connector

Pin #	Signal name	Direction[2]	Connector	Description
1	HGPIO10	I/O	J37	Spare Host GPIO
2	HGPIO11	I/O	J37	DataFlash Shutdown (DF_nSD)
3	HGPIO0	I/O	J37	Application LED (LED0)
4	HGPIO1	I/O	J37	Application LED (LED1)
5	HOST_nRESET	I/O	J37	Active low host reset
6	HGPIO8	I/O	J37	Temperature Sensor ADC (TEMP_SENSOR)
7	HGPIO9	I/O	J37	Spare Host GPIO
8	SER_UART1_nCTS	I/O	J37	Host UART1 Clear to Send
9	SER_UART1_nRTS	I/O	J37	Host UART1 Ready to Send
10	SER_UART1_TXD	I/O	J37	Host UART1 Transmit Data
11	SER_UART1_RXD	I/O	J37	Host UART1 Receive Data
12	HOST_nSS	I/O	J37	EZSP SPI Slave Select
13	HOST_SCK	I/O	J37	EZSP SPI Clock
14	HOST_MISO	I/O	J37	EZSP Master In-Slave Out
15	HOST_MOSI	I/O	J37	EZSP Master Out-Slave In
16	nHOST_INT	I/O	J37	EZSP Host Interrupt
17	VDD_3V_HOST	Power	J38	3.3V Connection
18	EZSP_UART2_nRTS	I/O	J38	EZSP UART Ready to Send
19	EZSP_UART2_nCTS	I/O	J38	EZSP UART Clear to Send

Pin #	Signal name	Direction[2]	Connector	Description
20	EZSP_UART2_RXD	I/O	J38	EZSP UART Receive Data
21	EZSP_UART2_TXD	I/O	J38	EZSP UART Transmit Data
22	HGPIO7	I/O	J38	Temperature Sensor Enable (TEMP_ENABLE)
23	HGPIO6	I/O	J38	Spare Host GPIO
24	HGPIO5	I/O	J38	Spare Host GPIO
25	HGPIO4	I/O	J38	Application Speaker (PIEZO)
26	HGPIO15	I/O	J38	DataFlash SPI Serial Out (DF_SO)
27	HGPIO14	I/O	J38	DataFlash SPI Serial In (DF_SI)
28	HGPIO13	I/O	J38	DataFlash SPI Clock (DF_SCK)
29	HGPIO12	I/O	J38	DataFlash SPI Chip Select (DF_nSS)
30	HGPIO3	I/O	J38	Application Button (BUTTON1)
31	HGPIO2	I/O	J38	Application Button (BUTTON0)
32	HOST_BTL	I/O	J38	Host Bootloader
33	NCP_nRESET	I/O	J38	Active low NCP reset
34	nWAKE	I/O	J38	EZSP SPI Wake
35	NC	N/A	J38	Not connected
36	GND	Power	J38	Ground connection

[2] with respect to the host

2.10 Prototyping Area

The 1.6" x 1.8" (0.1” pitch) prototyping area on the EM35x NCP Breakout Board offers software developers an extra degree of flexibility. As shown in Figure 4, it allows access to VBRD, GND, and 16 host GPIOs. Therefore, you can solder any sensor or input device to the prototyping area and connect it to the host GPIO for development and debugging.

As shown in Figure 8, the leftmost column is connected to GND and the rightmost column to VBRD. The top row is connected to the host GPIOs. Included in the top row are additional GND and JCLK connections. The remainder of the array is available for application development.

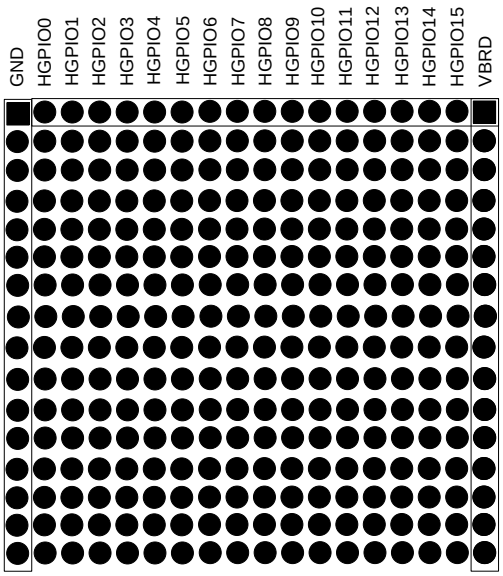


Figure 8. EM35x NCP Breakout Board prototyping area

3 EM35x NCP Breakout Board Schematic

The EM35x NCP Breakout Board schematic is included at the end of this document.

EM35X NCP Breakout Board

Sheet	Details
1	COVER SHEET
2	POWER MANAGEMENT, MANUFACTURING
3	APPLICATIONS CIRCUITS, BREADBOARD
4	EM35X RCM CONNECTORS, USER INTERFACES
5	HOST MODULE CONNECTOR, INTERFACES
6	SPI/UART MUX/DEMUX CIRCUIT
7	SPI/UART BLOCK DIAGRAM
8	REVISION NOTES

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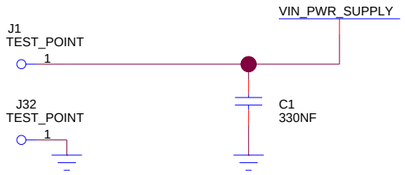
TITLE EM35X NCP BREAKOUT BOARD

PAGE COVER SHEET

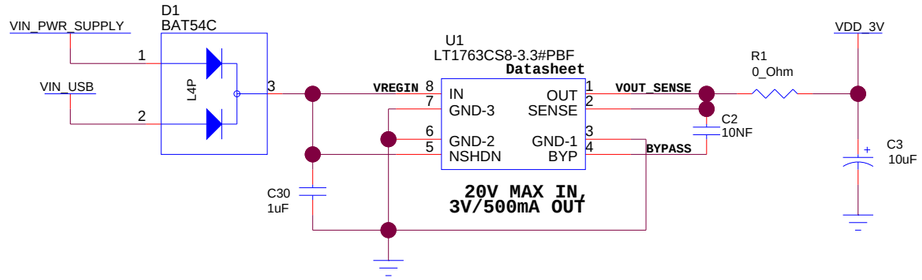
SIZE B DATE: 19-09-2010_22:13 SHEET: 1 of 8

POWER SUPPLY, DC, 4V to 20V

*** Place J1 close to J31**

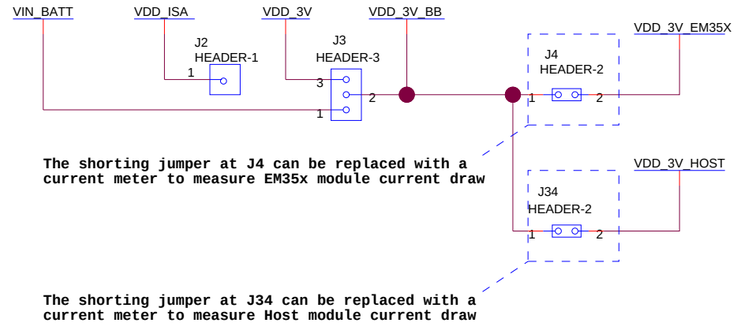


USB / VIN_PWR_JACK Down Conversion



Breakout Board and Module Power Selector

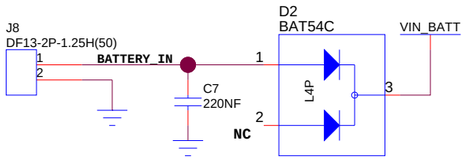
Headers J2 and J3 allow the user to select the power source.
There are five possible power sources for the Breakout board.
1. External 3V Supply (Connect directly to J3.2)
2. External Regulated supply from 4V to 20V (Connect shorting jumper between J3 pins 2.3)
3. Ember battery pack with 2 AAA (Connect shorting jumper between J3 pins 1.2)
2. USB Bus Powered (Connect shorting jumper between J3 pins 2.3)
4. Debug Adapter (Connect shorting jumper between J2 and J3.2)



BATTERY INTERFACE

Kit Provide Battery Pack for 2 AAAs, voltage range 1.5V to 3.1V

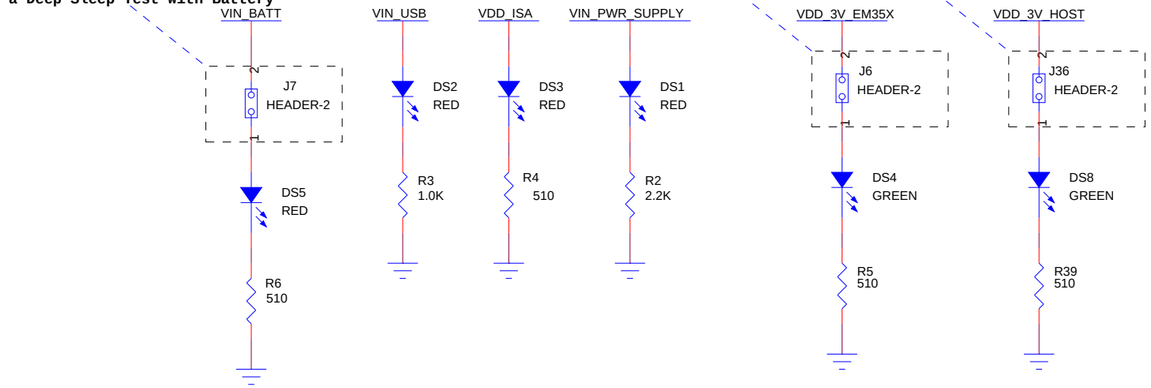
EM35x IC will not operate properly at voltages below 1.8V



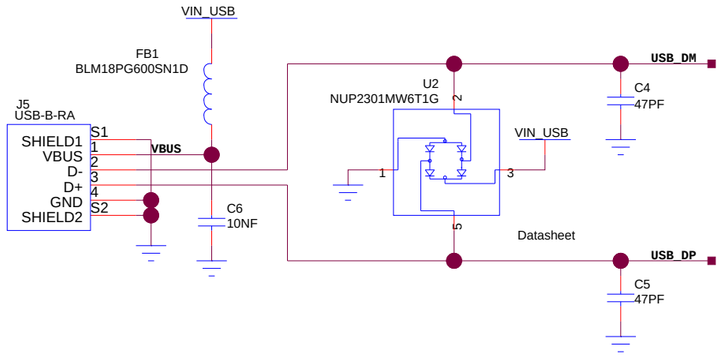
Power Indicator LEDs

*** Remove J67 when performing a Deep Sleep Test with Battery**

*** Remove J6, J36 when performing a Deep Sleep Test**

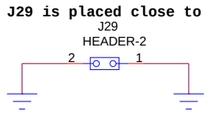


USB CONNECTION (TYPE B) 5V

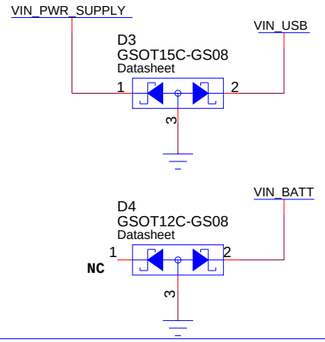


Test Equipment GND Connection

J29 is placed close to J41



ESD Suppression (Power Supply)



Shorting Jumpers

Place shorting jumpers across the following connector pins;

J2 and J3.2	**J33.2**
J4	**J33.4**
J6	**J33.6**
J7	**J33.8**
J9	**J33.10**
J10	**J33.12**
J11	**J34**
J12	**J35**
J13	**J36**
J14	**J39.1**
J15	**J40**
J16	**J42.1 and J42.2**
J17	**J42.3 and J42.4**
J25	**J42.5 and J42.6**
J26	**J42.7 and J42.8**
J27	**J42.9 and J42.10**
J28	**J42.11 and J42.12**
	J42.13 and J42.14

SHORTING JUMPER **X 35**

PCB Information

PCB1
710-0681-000

SN1
130-0681-000

Fiducials

FID1 FID2 FID3

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PAGE	**POWER MANAGEMENT, MANUFACTURING**	

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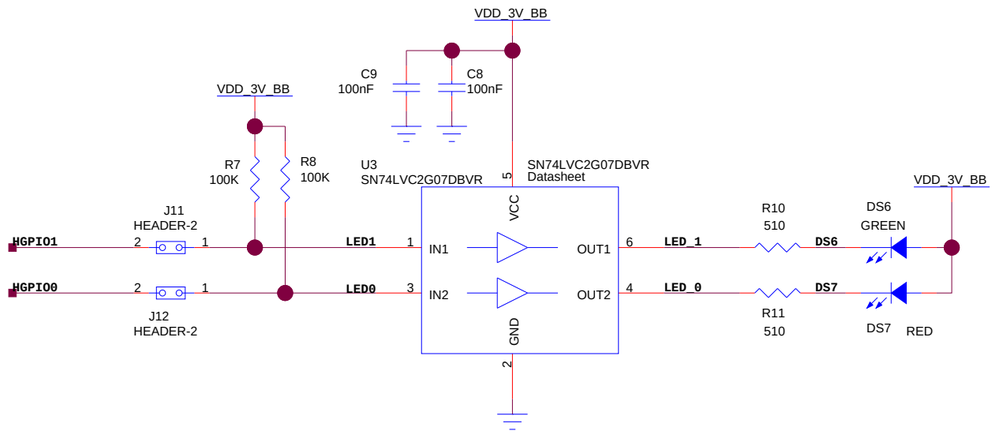
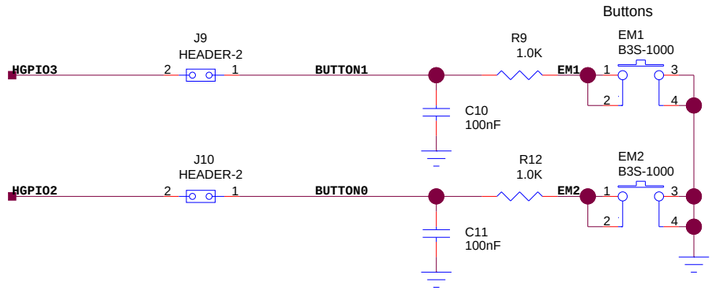
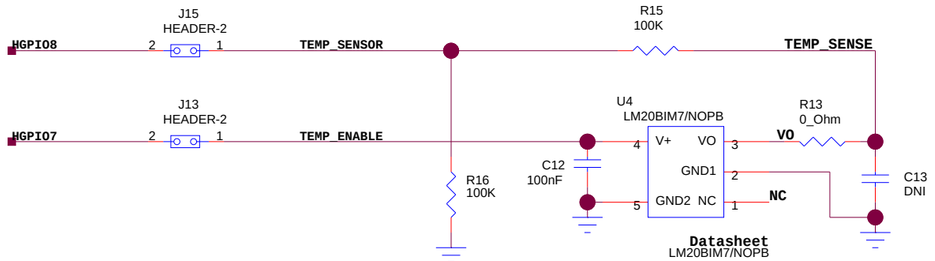
Host Application LEDs



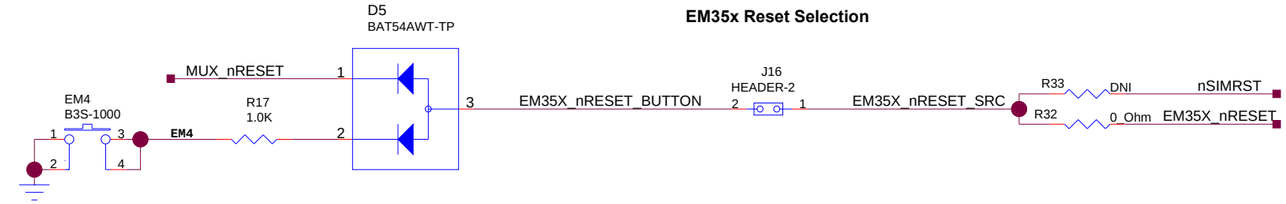
Host Application Buttons



Host Temperature Sensor

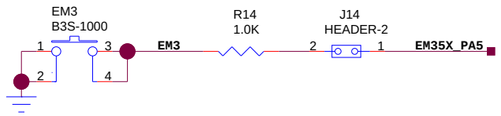


EM35x RESET Button (Active Low)

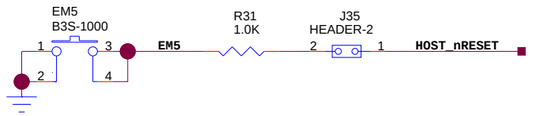


Host Piezo Speaker

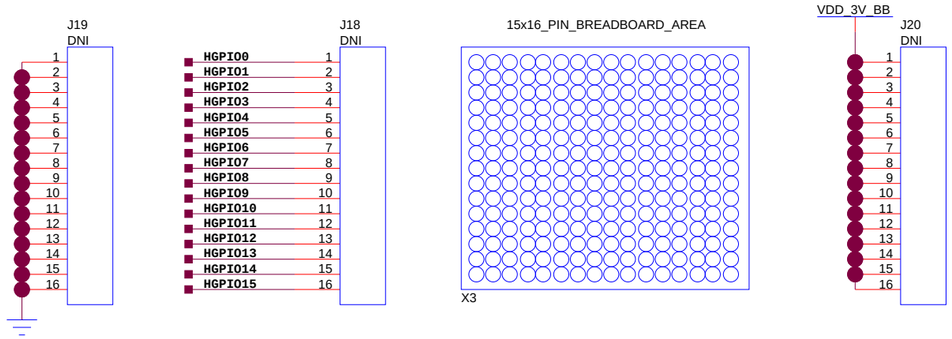
EM35x Bootloader Button (Active Low)



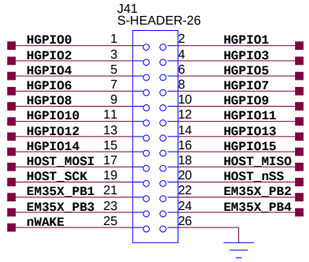
Host RESET Button (Active Low)



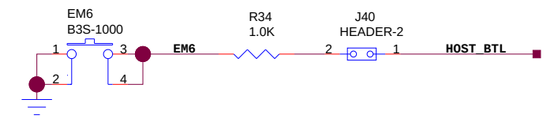
Peripheral Scratch Pad (0.1" pitch)



26-Pin, Dual Row Test Connector



Host Bootloader Button (Active Low)



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TITLE	EM35X NCP BREAKOUT BOARD
PAGE	APPLICATIONS CIRCUITS, BREADBOARD

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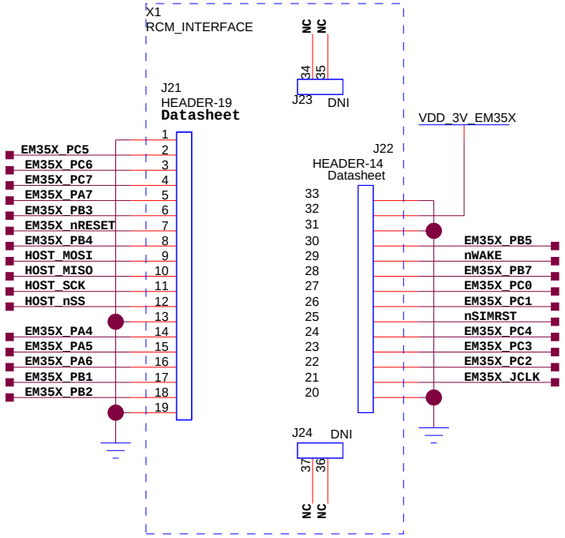
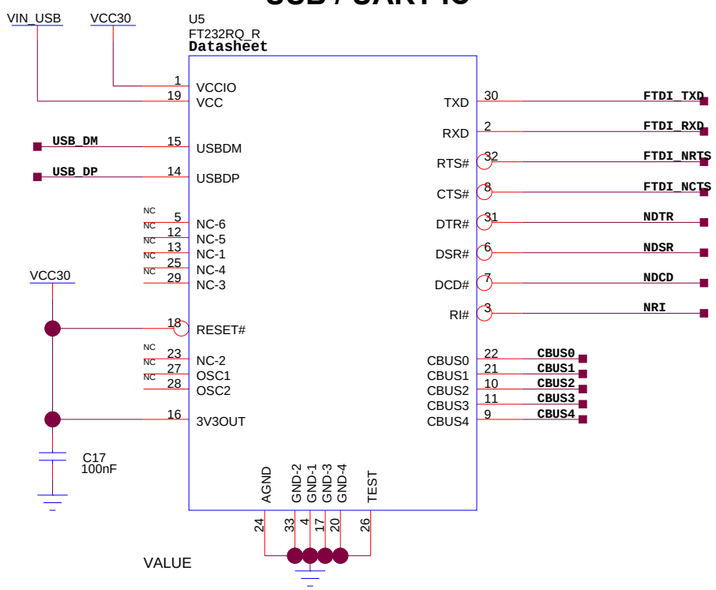
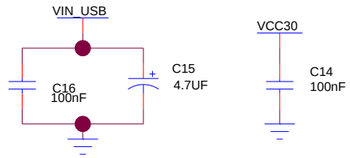
EM3XX RCM Interface Header



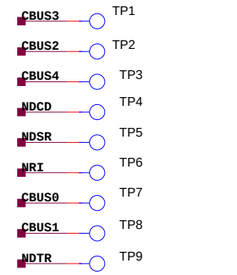
USB / UART IC



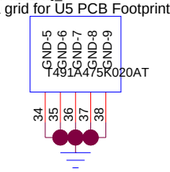
USB IC Decoupling



FTDi GPIO Test Points

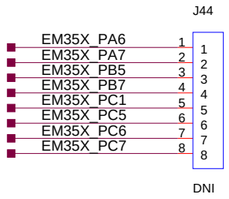


U5
FT232RQ_R
5 via grid for U5 PCB Footprint



EM35x GPIO Header

Access to unused EM35x GPIO

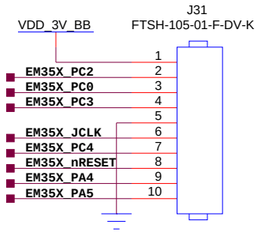


EM35x Packet Trace Port

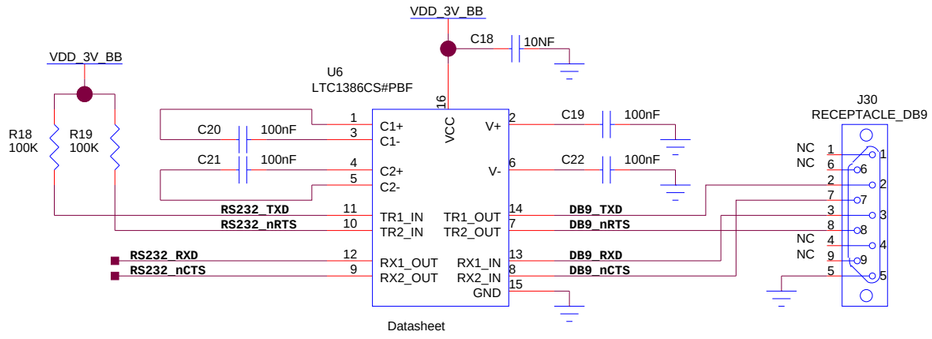
Datasheet

(Target Power)
(JTDO/SWO)
(nJRST)
(JTDI)

(JTCK/SWCLK)
(JTMS/SWDIO)
(nRESET)
(Packet Trace Frame)
(Packet Trace Data)

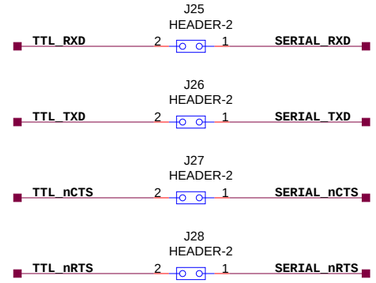


TTL to RS-232 Transceiver

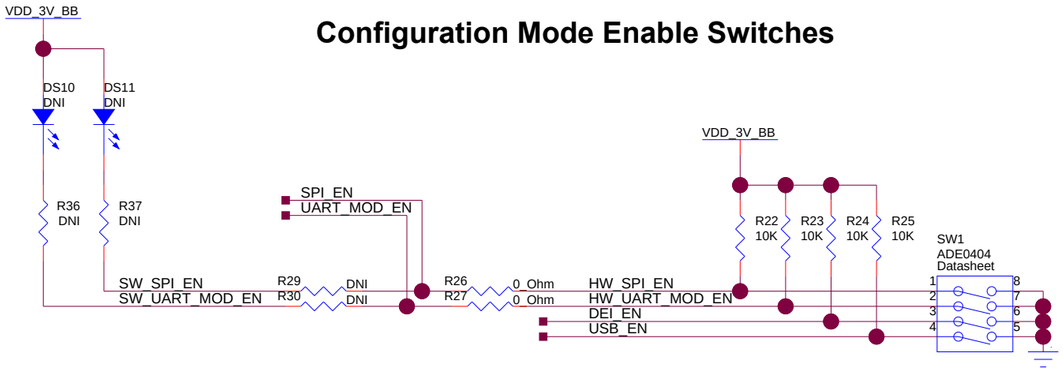


TTL Signal Access

FROM DEI/TTL MUX <--- ---> TO USB/232 MUX



Configuration Mode Enable Switches



Software/Hardware Enable

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PAGE	EM35X RCM CONNECTORS, USER INTERFACES	

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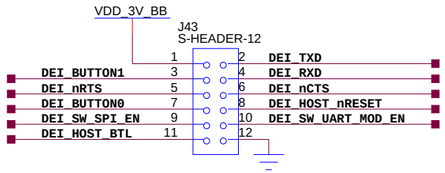
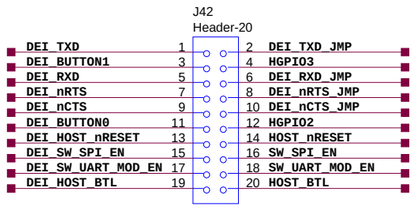
Host DEI

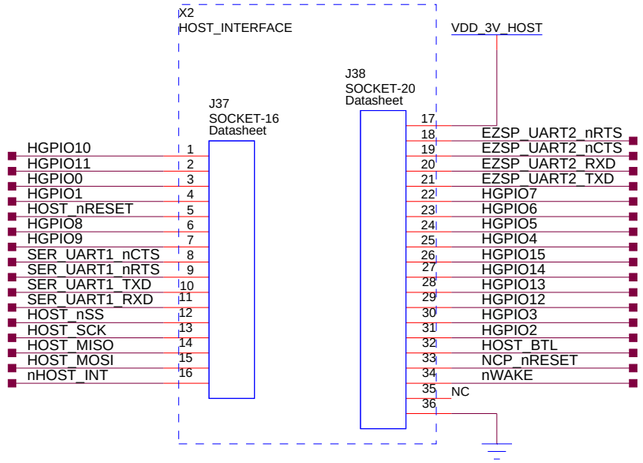


Host DEI Jumpers

Should be placed near J43



Host Module Interface Headers



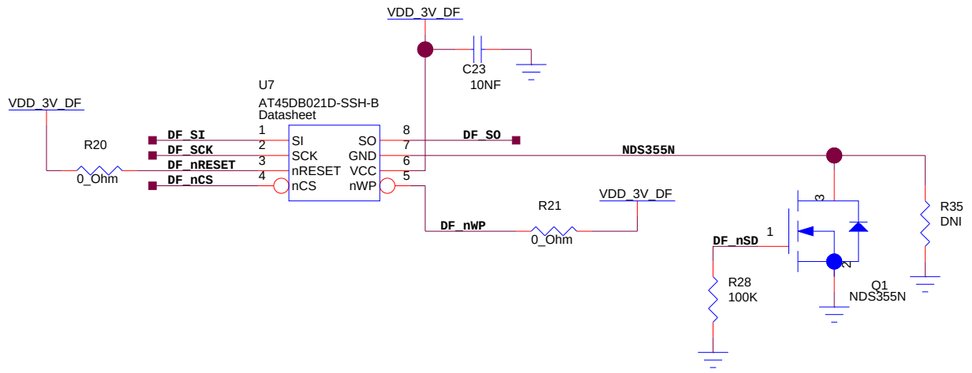
J37p35 - NC, available for later use

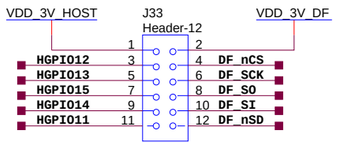
Host Module Application Peripheral GPIO Mapping

HOST_NET_NAME	GPIO FUNCTION
HGPIO0	Application LED (LED0)
HGPIO1	Application LED (LED1)
HGPIO2	Application Button (BUTTON0)
HGPIO3	Application Button (BUTTON1)
HGPIO4	Application Speaker (PIEZO)
HGPIO5	Spare GPIO
HGPIO6	Spare GPIO
HGPIO7	Temperature Sensor Enable (TEMP_ENABLE)
HGPIO8	Temperature Sensor ADC (TEMP_SENSOR)
HGPIO9	Spare GPIO
HGPIO10	Spare GPIO
HGPIO11	DataFlash Shutdown (DF_nSD)
HGPIO12	DataFlash SPI Chip Select (DF_nCS)
HGPIO13	DataFlash SPI Clock (DF_SCK)
HGPIO14	DataFlash SPI Serial In (DF_SI)
HGPIO15	DataFlash SPI Serial Out (DF_SO)

DataFlash (SPI Interface with Host)

Voltage range of the AT45DB021D is 2.7V to 3.6V
Radio Modules which are expected to operate at voltages below 2.7V will require a DC to DC up-converter supply source for the AT45DB021D
Input data on SI is always latched on the rising edge of SCK
Output data on SO is always clocked out on the falling edge of SCK





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PAGE	HOST MODULE CONNECTORS, INTERFACES	

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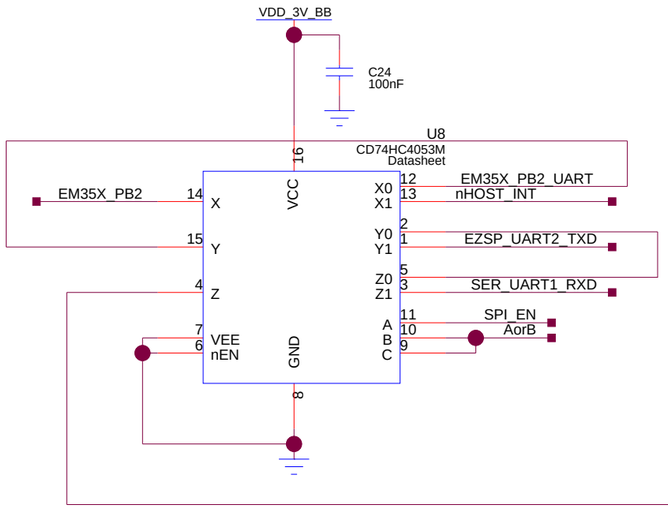
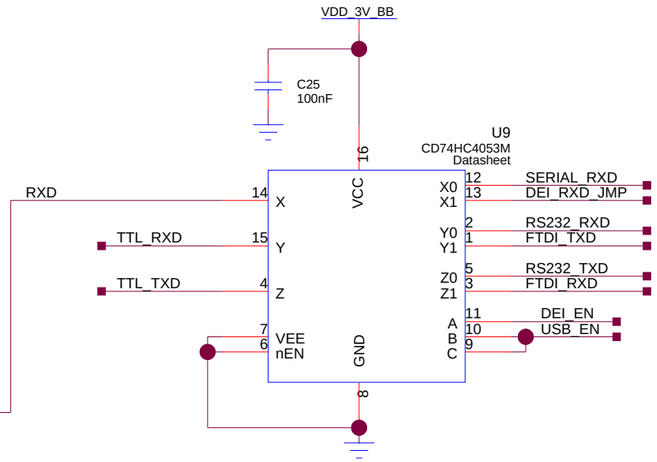
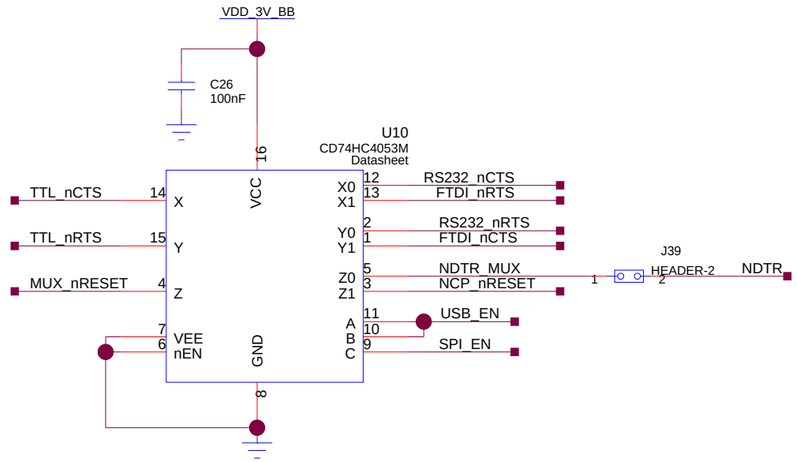
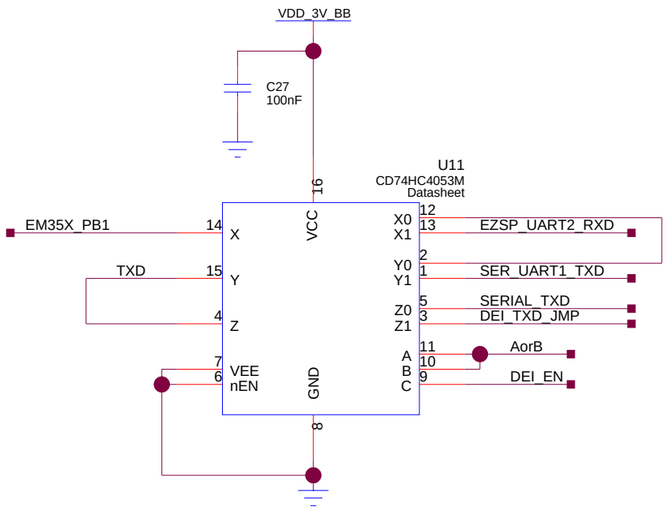
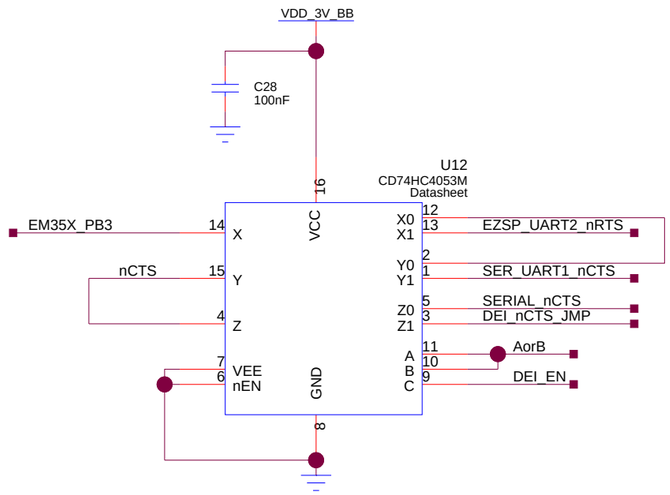
SPI/UART Multiplexer/Demultiplexer Circuit

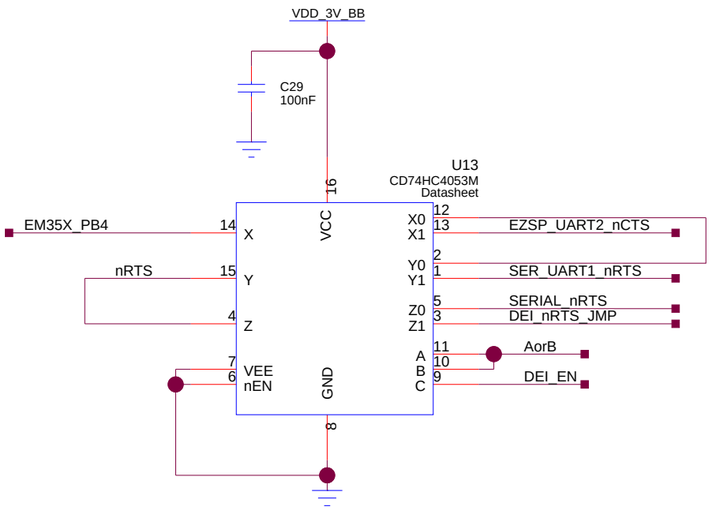




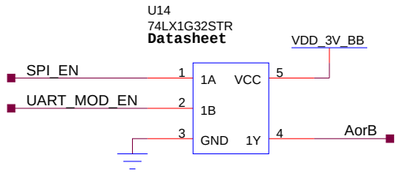








SPI_EN (A) or UART_MOD_EN (B)



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TITLE	EM35X NCP BREAKOUT BOARD	
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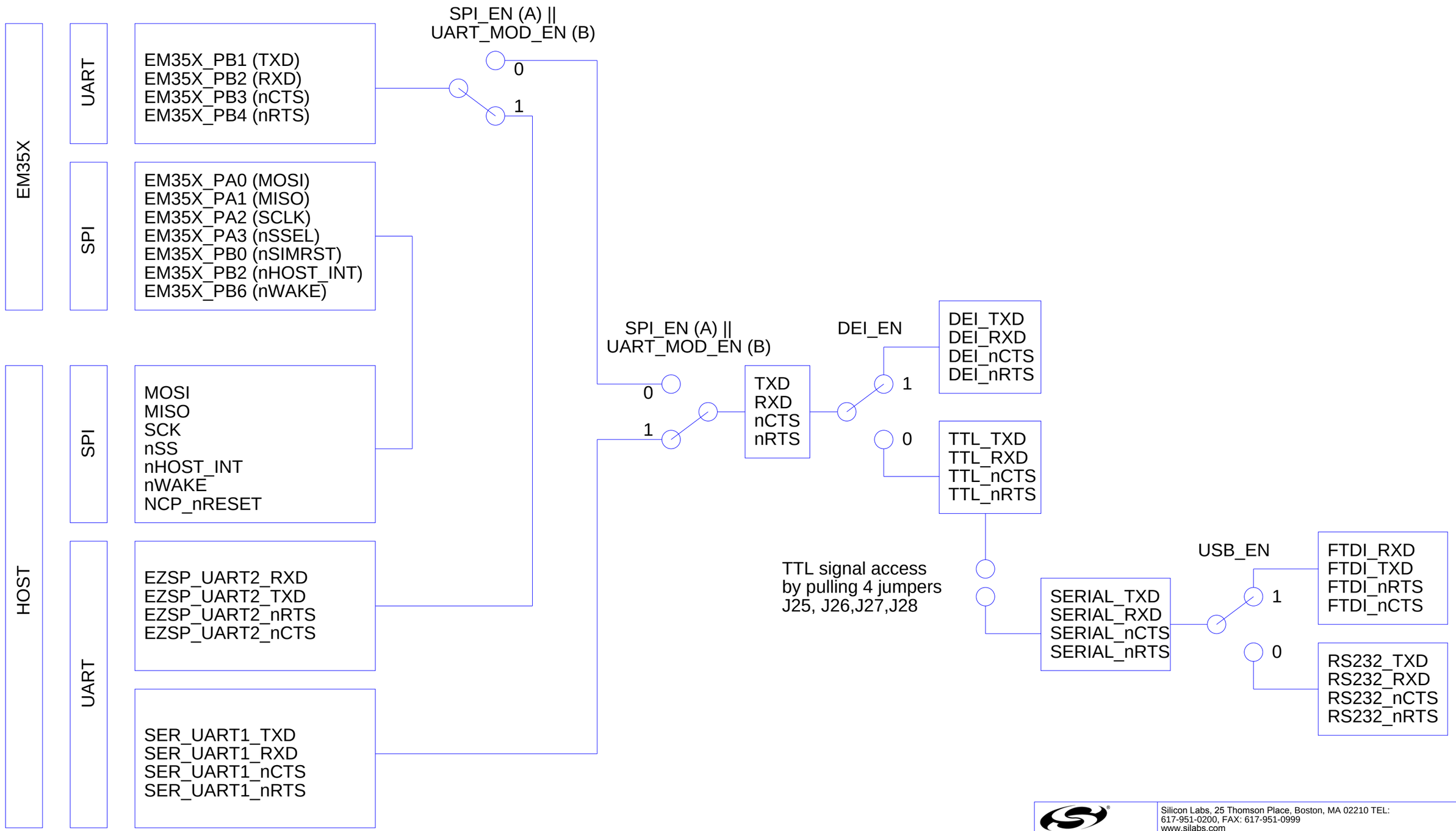

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DWG	**SCH0681**	REV **A0**
TITLE	**EM35X NCP BREAKOUT BOARD**	
PAGE	**SPI/UART BLOCK DIAGRAM**	

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SCHEMATIC NOTES:

-- Version P0 --
*Released: 2010-06-11
*Initial version released, Version P0 (initial draft)

-- Version A0 --
*Released: 2010-09-20
*Production version release
*Changes from P0 to A0:
1) Swapped UART1 nets with UART2 nets based on changes for UART1 STM32 BTL.
2) Renamed UART1 nets to SER_UART1_TXD, etc.
3) Renamed UART2 nets to EZSP_UART1_TXD, etc.
4) Updated sheet 7 chart for UART changes.
5) Added SJ34-35 for J7 and J33.12.
6) Removed SW_DEI_EN and DEI_SW_DEI_EN (DS9, R28, R35, R38).
7) Updated J43p11 from DEI_SW_DEI_EN to DEI_HOST_BTL.
8) Updated J42p19/20 from DEI_EN to HOST_BTL.
9) Symbol clean-up for using PART_NUMBER rather than Manufacturer P/N.
10) Replaced 570_0603_100 with _101, and _400 with _401.
11) Added Q1 shutdown transistor circuit for DataFlash.
12) Changed title block text from EZSP to NCP to reflect product name.
13) Corrected 500_4053_001 symbol due to error with Ember P/N (-000 instead of -001).
14) Added 1uF cap to input of regulator U1.
15) Changed C3 from 554-106A-016 (ESR 7 ohm) to 554-106A-020 (ESR 1 ohm).

PCB LAYOUT NOTES:

-- Version P0 --
*Released: 2010-06-11
*Initial version released, Version P0 (initial draft)

-- Version A0 --
*Released: 2010-09-20
*Production version release
*Changes from P0 to A0:
1) Schematic changes reflected in layout.
2) Corrected J41p15 SST error (was HGPIO1 instead of HGPIO14).
3) Added pin1 marking for U7 SST.
4) Corrected board outline dimensioning error.
5) Added bump-on outlines in SSB and ASB.
6) Corrected D5 decal error (was SOT23 instead of SOT323).
7) Updated LED0603 decal with Cathode C marking.
8) Test point coverage for nets without probe access.

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TITLE	EM35X NCP BREAKOUT BOARD	
PAGE	REVISION NOTES	

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CONTACT INFORMATION

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